UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,850	07/15/2003	Yukio Tanaka	0756-7177	4342

31780 7590 12/18/2006

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
NHU, DAVID	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
12/18/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Suppl.

Notice of Allowability	Application No.	Applicant(s)	
	10/618,850	TANAKA ET AL.	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/26/06*.

2. ☒ The allowed claim(s) is/are *8-37*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *10/295,886* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

1. Claims 8-37 allowed.

2. The following is an examiner's statement of reasons for allowance: None of the references of record teaches or suggests as cited in claims 8, 14, 20, 26, 32: introducing a first impurity element into portions of the first and second semiconductor layers so as to form a pair of first impurity regions with a channel formation region interposed therebetween; introducing a second impurity element into portions of the first and second semiconductor layers so as to form a pair of second impurity regions with the pair of first impurity regions interposed therebetween; and introducing a third impurity element into portions of the first semiconductor layer so as to form a pair of third impurity regions with the pair of second impurity regions interposed therebetween, wherein an edge of the gate insulating film is aligned with a boundary between the pair of second impurity regions and the pair of third impurity regions (as cited in claim 8); introducing a first impurity element into portions of the first and second semiconductor layers so as to form a pair of first impurity regions with a channel formation region interposed therebetween; introducing a second impurity element into portions of the first and second semiconductor layers so as to form a pair of second impurity regions with the pair of first impurity regions interposed therebetween; introducing a third impurity element into portions of the first semiconductor layer so as to form a pair of third impurity regions with the pair of second impurity regions interposed therebetween (as cited in claim 14); introducing a first impurity element into portions of the first and second semiconductor layers so as to form a pair of first impurity regions with a channel formation region interposed therebetween; introducing a second impurity element into portions of the

first and second semiconductor layers so as to form a pair of second impurity regions with the pair of first impurity regions interposed therebetween; introducing a third impurity element into portions of the first semiconductor layer so as to form a pair of third impurity regions with the pair of second impurity regions interposed therebetween; and forming wirings so as to be in contact with the pair of third impurity regions, wherein an edge of the gate insulating film is aligned with a boundary between the pair of second impurity regions and the pair of third impurity regions (as cited in claim 20); introducing a first impurity element into portions of the first and second semiconductor layers so as to form a pair of first impurity regions with a channel formation region interposed therebetween; introducing a second impurity element into portions of the first and second semiconductor layers so as to form a pair of second impurity regions with the pair of first impurity regions interposed therebetween; introducing a third impurity element into portions of the first semiconductor layer so as to form a pair of third impurity regions with the pair of second impurity regions interposed therebetween; and forming wirings so as to be in contact with the pair of third impurity regions (as cited in claim 26); introducing a first impurity element into portions of the first and second semiconductor layers so as to form a pair of first impurity regions with a channel formation region interposed therebetween; introducing a second impurity element into portions of the first and second semiconductor layers so as to form a pair of second impurity regions with the pair of first impurity regions interposed therebetween; introducing a third impurity element into portions of the first semiconductor layer so as to form a pair of third impurity regions with the pair of second impurity regions interposed therebetween; and forming wirings so as to be in contact with the pair of third impurity regions, wherein an edge of the gate insulating film is aligned

with a boundary between the pair of second impurity regions and the pair of third impurity regions (as cited in claim 32).

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Tanaka et al (6,635,505 B2): Method of Manufacturing an Active Matrix Type Semiconductor Display Device.

5. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu , (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM.

The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.

David Nhu

December 11, 2006

DAVID NHU
PRIMARY EXAMINER